International Journal of Recent Engineering Science
ISSN: 2349-7157/ https://doi.org/10.14445/23497157/IJRES-V12I2P106

Volume 12 Issue 2, 46-57, Mar-Apr 2025


*Original Article*

# Design and Simulation of Fault Diagnosis Methods for Multilevel Inverters Used in Smart Grid Technologies

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Received: 12 February 2025 Revised: 14 March 2025 Accepted: 30 March 2025 Published: 14 April 2025

***Abstract*** *- The advanced control mechanisms of the smart grid system optimize energy efficiency and power generation. Most faults found in the control systems and their power components may cause a ripple effect throughout the entire system, thus raising a serious concern for reliability. The study highlights the development of fault identification techniques for three-phase multilevel inverters, an important element of smart grid technology. These kinds of inverters are constructed using several power electronic components, which may include MOSFETs or power diodes, and they provide a very high-quality AC voltage to the power system. As the number of levels increases, the AC signal gets more pure; therefore, fault detection in these inverters is critical to avoid disruptions in the system. Different techniques for detecting faults are presented, including analyzing stator currents, current and voltage sensors, identification of single and multiple switching faults, and voltage anomalies associated with transducers malfunctioning. An additional aspect of the research is the development of adaptable multilevel converter models that can be customized for the various layouts of converter topologies. The actual detection techniques display application using harmonic analysis and FFT analysis under simulation environments representing normal operating conditions, failure of isolated power components, and short-tripping scenarios.*

***Keywords*** *- Converter topology layouts, Harmonic analysis, Multilevel inverters, Power electronic components, Smart grid.*

## 1. Introduction

The smart grid is changing all energy networks by embedding the smart devices that facilitate communication flow bi-bidirectionally from traditional electricity networks to consumers and consumers to the grid operators. It is a key strategic initiative in keeping energy efficient and optimizing renewable energy generation power that provides value to top-tier energy providers.

Multilevel inverters are at the core of smart grids. Advanced switching techniques are needed to enhance low-voltage power to higher voltage and current levels. This presents a bright future because of the inherent limitations that current power semiconductor technologies present against multilevel inverters. Electronic switch failures pose challenges to voltage distortions [1], current fluctuations, and overall instability of the system.

There are a lot of fault-detection schemes that impose overall reliability, like monitoring inverter voltage [2,3], current values [4], and analyzing Fast Fourier Transform (FFT) patterns output voltage with respect to faults identifying [5,6]. Observing the Total Harmonic Distortion (THD) is essential because the THD levels show how serious the faults caused by deviations of stepped voltage and current outputs may be. Despite all these merits, the approaches noted above still suffer some drawbacks.

The main focus of this paper is the fault diagnosis scenarios for three-phase multilevel inverters in smart grid technologies. It emphasizes diagnosis for isolated power electronic converters, MOSFET component configurations short-circuit conditions [7], detecting single, double, or triple-switching failures [8], and observing the THD values. The proposed simulation model can effectively differentiate these faults by investigating voltage and current variations in different operation conditions, thus proving its potential to contribute to fault diagnosis in smart grid applications.

There are more effective and advanced methods that could be used for real-time fault detection like, Robust Intelligent and Adaptive Detection Mechanisms in the smart grid environment, Artificial Intelligence data analysis, further research on the Optimal of numbers of levels in Multilevel Inverter (MLI), and Switched Capacitor (SC) inverters.

## 2. Literature Review

Ji et al. (2022) [1], This work proposed a highly strong detection mechanism for open-switch faults in grid-connected inverters. The proposed method improves by

combining signal processing techniques with intelligent detection algorithms. They strive for better system reliability while tackling the comparatively common failure modes of power electronics that require continuous operation in smart grid applications. These results demonstrate that the approach can classify different fault types with considerable classification purity in terms of low false detection rates, thus making it a highly viable solution for industrial applications.

Kouro et al. (2010) [2], The author's extensive overview of multilevel connector topologies, control strategies, and their industrial applications includes different control techniques, primarily Space Vector Modulation (SVM) and Pulse-Width Modulation (PWM) to improve power quality and efficiency. It highlights how the advantages of multilevel converters on high-power applications, such as electric drives, renewable energy systems, and HVDC transmission, do not come without challenges, such as higher component numbers and control complexities. Proposed solutions against these drawbacks are also given in the study.

Orfanoudakis et al. (2010) [3], The study compares the available power losses of three-level inverter and two-level inverter topologies under various operating conditions. In this regard, the research employs analytical models and results from simulation-based tests to quantify loss through conduction and switching. Moreover, it shows that three-level inverters are more efficient due to less voltage stress and harmonic distortion. The results especially impact areas of renewable energy applications, electric vehicle drives, and efficiency gains, which could mean a lot of savings in terms of energy.

Rodriguez et al. (2002) [4], The work that started the field, this exhaustive survey treats multilevel inverter technology, such as cascaded H bridge, diode clamped, and capacitor clamped topologies. It also discusses various modulation and control techniques, from selective harmonic elimination to carrier-based PWM, and how well these techniques minimize Total Harmonic Distortion (THD). Furthermore, this paper examines new emerging applications in FACTS devices, industrial motor drives, and grid-connected renewable energy systems, thus serving as a research fund for future investigations into multilevel inverters.

Prejbeanu et al. (2020) [5], A homology study of fault detection techniques for multilevel inverters is generated using simulation models. The authors also propose a diagnostic procedure based on harmonic analysis and machine learning algorithms for detecting and classifying faults in real time. This methodology takes fault detection alarm reliability for smart grid applications to another level by reducing false alarms and improving fault isolation. Results prove intelligent fault monitoring feasibility at large-scale power networks.

Lezana et al. (2009) [6], The novel fault detection method applies to multi-cell converters based on the output voltage frequency analysis. The major premise is that prompt fault detection can be accomplished by finding deviations in voltage spectra, thus minimizing downtime and preventing the possibility of great failure. So, the study suggests an inbuilt gain of spectral analysis over time domain approaches in a finding that may, particularly in power conversion systems, exhibit effectiveness in identifying hardware degradation or even intermittent faults.

Sivakumar et al. (2014) [7], The study aims to develop a hybrid framework for at-the-fault diagnosis that employs Artificial Neural Networks (ANN) as well as Discrete Wavelet Transform (DWT). The fault being diagnosed is a short switch fault in cascading H-bridge multilevel inverters. The signals coming out of the inverter have been analyzed using DWT to get their transient characteristics, and ANN has been deployed to classify fault conditions in a highly precise way. Therefore, this is expected to greatly increase the accuracy of fault identification.

Estima and Cardoso (2013) [8], a new algorithm for real-time diagnosis of simultaneous open circuit faults in voltage-fed PWM motor drives using reference current errors is presented in this paper.

The algorithm can diagnose the faults in real time without additional sensors, which makes it cost-effective for application in industrial motor drives. The experimental results validating the method show its effectiveness in distinguishing fault conditions from normal operation variation.

Labrador Rivas and Abrão (2020) [9] This article comprehensively reviews fault monitoring techniques used in smart grids. It emphasizes artificial intelligence and data-driven methods that the authors categorize faults; symmetrical and asymmetrical kinds are analyzed against state-of-the-art detection methodologies such as wavelet transforms, machine learning, and deep learning techniques. The study reveals how beneficial such smart fault detection would be in continuing to build better resilience and reliability into the grid.

R. Beniak, K. Rogowski (2016) [10], This is the main presentation of a proposed optimization switching method suggested for three-level Neutral-Point-Clamped (NPC) inverters that minimize switching losses.

The proposed method modifies the switching sequence improves the dissipated power without compromising output voltage quality. The attained results suggest that greater efficiency, especially for high-frequency operations, could be translated into an industrial motor drive or renewable energy converter application.

Nabae et al. (1981) [11] This paper represents the major work in power electronics that proposed the Neutral Point-Clamped (NPC) PWM inverter topology, thus maintaining the total harmonic distortion appreciably low in comparison to conventional level two inverters. The NPC inverter improves the quality of the voltage waveform and increases efficiency in high-power applications such as industrial drives and HVDC transmission. This work provided a basis for contemporary research on multilevel inverters.

Sarita et al. (2021) [12], The authors propose an open circuit fault diagnosis framework in multilevel inverters applying a Support Vector Machine (SVM) derived classification technique. The detection algorithm extracts fault signatures from the inverter output signals that are classified using SVM, achieving high accuracy in fault identification.

These research works have contributed substantially to developing multilevel inverter technologies, methods for fault detection, and efficiency optimization strategies. Specifically, they deal with pertinent topics such as fault diagnosis with artificial intelligence, spectral analysis, machine learning, and optimization switching techniques for converter efficiency improvements.

## 3. Technical Reviews

Load control, an advanced control system, is in charge of reinforcing the existing electrical supply network in a smart grid for good efficiency and reliability. Smart grid technology takes the intelligent distribution network in full gamut from control centers to power equipment to renewable energy sources and to sensors, converters, storage systems, and communication infrastructures, modern as well as conventional. The system uses digital control technology to provide optimized electricity distribution while efficiently accommodating renewable energy sources.

The intelligent electronic networking system creates real-time direct communication among end users. Therefore, if one component experiences power disruption, it will not disturb the entire network. Fault management of smart grid technology is presented in Figure 1 in the topology. In case of a load fault, the faulty circuits will be the ones isolated, and only specified industrial or commercial loads will be disconnected.

Industrial loads, particularly motor drives, are prone to faults due to electrical, mechanical, or perceptual nature [9]. Some inverter faults, among stator faults or electrical faults, may be attributed to short circuits or open circuits.

Inverters widely exist in smart grids as voltage supply sources for power electronic devices and control centres of subsystems. Inverters are affected by transient disturbances, however. The multilevel Sinusoidal Pulse Width Modulation [SPWM] of the inverter type relies on several carrier-modulating signals [10], thus increasing the odds of failure of MOSFETs and transistors. The failures affect both the line voltage phase and load of the inverter, with high distortion values leading to high THD.

Higher inverter levels produce signals that more closely resemble the pure sinusoidal waveform, reducing distortion and, by extension, THD. Multi-carrier modulation techniques have been developed to tackle the problems of minimizing voltage variation across different inverter levels. However, the ordinary SPWM with triangular carriers also suffers from some current distortion.

The three-level multilevel inverter, represented in Figure 2 and called in literature a diode-clamped multi-level inverter or NPC inverter, was first presented by Nabae [11]. This configuration has four switches for each phase leg and two diodes interconnecting the capacitor's neutral midpoint.

Table 1 summarizes the different switching states and their respective output voltage values across two phases of the multi-level DCMI. Compared to conventional two-level inverters, the NPC design adds a zero-voltage level, resulting in a three-level output voltage. Activating a transistor provides an output of 1, and deactivating one gives 0, while clamped diodes maintain the intermediate zero voltage state.

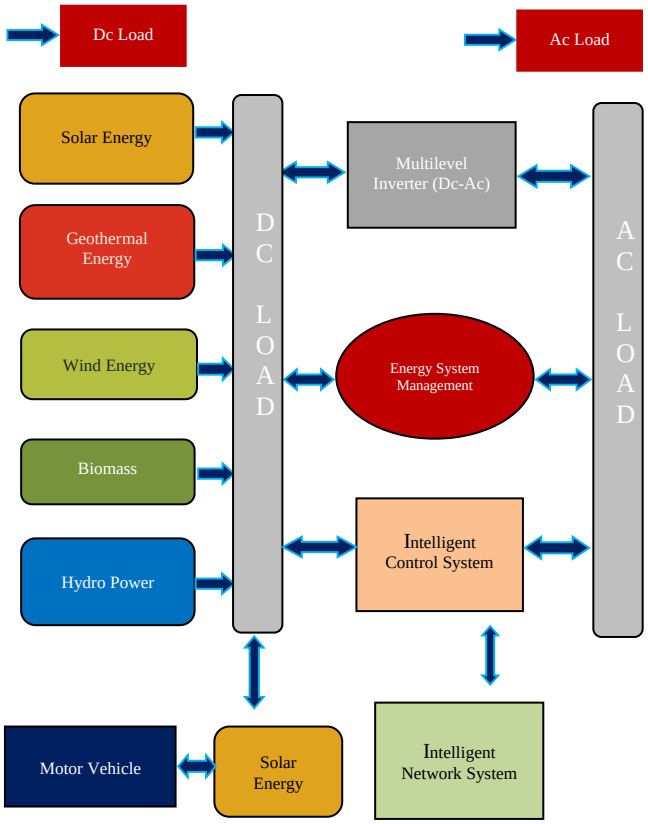


**Fig. 1 Topology of smart grid technology**

**Table 1. Various switching arrangements and corresponding output voltages**

| $S_{a1}$ | $S_{a1'}$ | $S_{a2}$ | $S_{a2'}$ | $S_{b1}$ | $S_{b1'}$ | $S_{b2}$ | $S_{b2'}$ | $V_{a0}$ | $V_{b0}$ | $V_{ab}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | $\frac{-V\mathrm{dc}}{2}$ | $\frac{V\mathrm{dc}}{2}$ | $-V_{dc}$ |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | $\frac{-V\mathrm{dc}}{2}$ | 0 | $\frac{-V\mathrm{dc}}{2}$ |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | $\frac{V\mathrm{dc}}{2}$ | $\frac{V\mathrm{dc}}{2}$ | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | $\frac{-V\mathrm{dc}}{2}$ | $\frac{-V\mathrm{dc}}{2}$ | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | $\frac{-V\mathrm{dc}}{2}$ | $\frac{V\mathrm{dc}}{2}$ |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $\frac{V\mathrm{dc}}{2}$ | $\frac{-V\mathrm{dc}}{2}$ | $V_{\mathrm{dc}}$ |

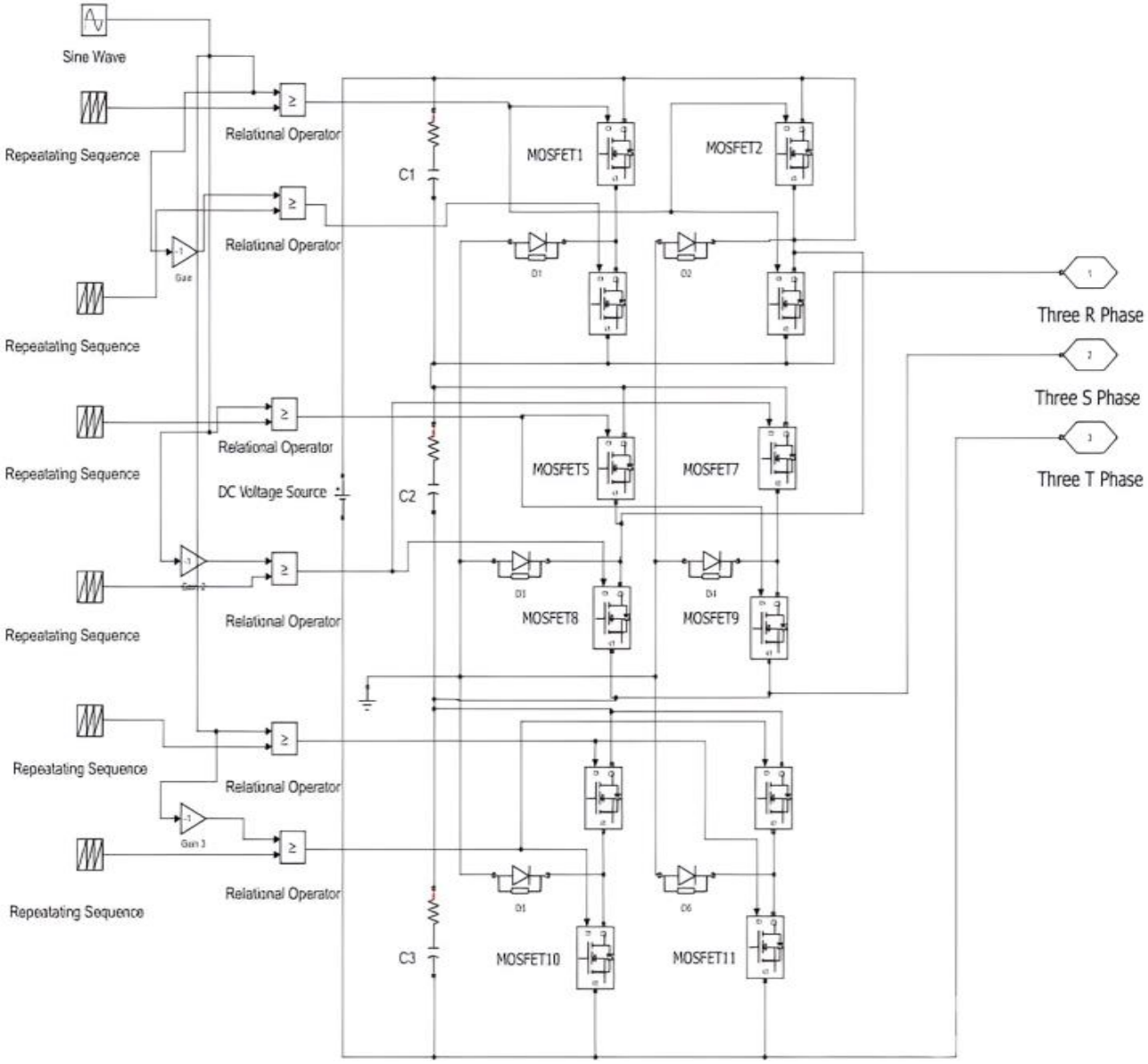


**Fig. 2 Configuration of DCMI inverter topology**

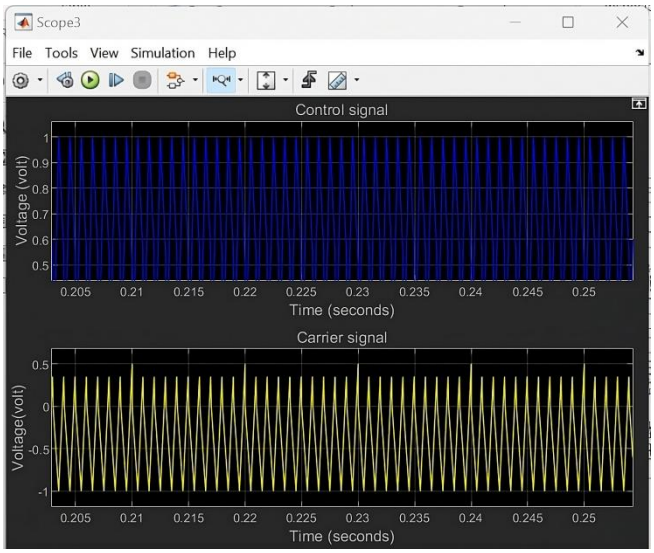


**Fig. 3 The graph above illustrates the control signal (up) and carrier signal (down)**

The p-q theory is known to be founded by research done by Akagi, which is instantaneous power theory [10]. Clarke transformation, also called α-β-0 transformation, is the name given to the principle using a real matrix to transform three-phase voltages and currents into (α-β-0) stationary reference frames. This transformation becomes a necessary element in an active power filter monitoring system for assessing the performance of a three-phase inverter on issues of reactive power, harmonic distortion, and system imbalance. In this regard, Figure 3 answers with multi-carrier control signals.

## 4. Methods of Control

In these automatic motor systems, synchrony is very important, but there is just a small glitch in the control that can lead to catastrophic failure. Hence, the transducers play a vital role in observing processes and anomalies in control signals or measurements. In this scenario, even a single erroneous or misleading data from the transducers can make the entire system fall apart. In such a highly sensitive area, as far as the Smart Grid networks are concerned, predicting and preempting the occurrence of faults in the future becomes imperative. One single misstep would have ramifications, which would make proactive fault detection an issue of paramount importance.

### *4.1. Detecting Voltage Sensor Malfunction*

In normal operation, the discrepancy between DC links is supposed to maintain a sufficiently narrow margin. When there is a malfunction in a voltage sensor, the impact is quite devastating. Such an event may be sudden and catastrophic or gradual and unnoticed. In the first case, a sudden voltage spike triggers an emergency shutdown and prevents the detection of multi-period sampling errors. In the second, the voltage error slowly creeps up while the motor system continues operating during the growth of the fault.

It is necessary to design a very reliable fault detection strategy to avoid succumbing to these failures. In the first case study, the threshold voltage limit can be defined by the buffer zone around the limit. If the difference between the present voltage value and the previous measurement exceeds this threshold, then a defect in a voltage sensor can be isolated immediately. However, such a criterion is ineffective for cases where voltage error behaves erratically or fluctuates very quickly. The hallmark of the model in the second case study that leads to diagnosing a voltage sensor failure is the appearance of a strong ripple voltage in the feedback voltage $U_{fdk}$ at the occurrence of the sensor failure. This disturbance ripples out its effects onto the magnetic fields in small positive and negative vectors. These vectors may cause high-frequency rippling in the voltages, unbalancing the capacitor voltage, and voltages could even be split into positive and negative components.

To tell between faults within the voltage sensor and that in the DC link, the voltage difference ΔU would be given by the equation $\Delta U = (U_{ref} - U_{fdk})$. When the voltage sensor is faulty right in the middle, the value of ΔU is constant. If the fault lies inside the DC link, the ripple will be seen in ΔU, affecting the output voltage. By analyzing the fast transient change in the output signal of the voltage comparing tool, high-frequency voltage ripple U can be analyzed to yield a fault on the voltage sensor by a corresponding deviation of ΔU.

$$\begin{matrix} u_a \\ u_b \\ u_c \end{matrix} = V \begin{bmatrix} sin(\omega_s t \\ sin(\omega_s t - \frac{2\pi}{3}) \\ sin(\omega_s t - \frac{4\pi}{3}) \end{bmatrix} \quad (1)$$

$$u_d = R_s + L_d \frac{di_d}{dt} - \omega_s L_q i_q \quad (2)$$

$$u_q = R_s i_q + L_q \frac{di_d}{dt} + \omega_s L_d i_d + \omega_s \psi_f \quad (3)$$

$$u_{feedback} = \sqrt{u_{d^2} + u_{q^2}} \quad (4)$$

### *4.2 Detecting Speed Sensor Malfunction*

When a DC or AC load creates an over-current or a fault, the supply network will disperse. The embedded storage systems and protective systems isolate failing loads. In three-phase isotropic motor drive units, a speed sensor measures the velocity and location of the rotor. One of the most critical failures in this system is the loss of sensor signal. When the failure occurs, the calculated speed drops to zero within a very short time, whereas the actual speed of the rotor rises to the maximum limit under the influence of the DC link voltage. The following rotor angular velocity expression:

In this respect, $\lambda_T$ stands for the torque angle, whereas λs denotes the stator flux angle. The flowchart depicting the entire process is shown in Figure 4.

In that, s means rotation of the stator flux, and T implies velocity w.r.t. rotor. Under steady-state conditions, $\lambda_T$ will remain constant, hence $\upsilon_T$=0. Because of the low torque recovery rate, $\upsilon_T$ is not important during dynamic conditions; therefore, estimating the rotor angular speed from the rotational velocity of the stator flux is an efficient way.

$$\boldsymbol{v_{ef} = \frac{d\theta}{dt}(\lambda_s + \lambda_T) = v_s + v_T \sim v_s} \quad (5)$$

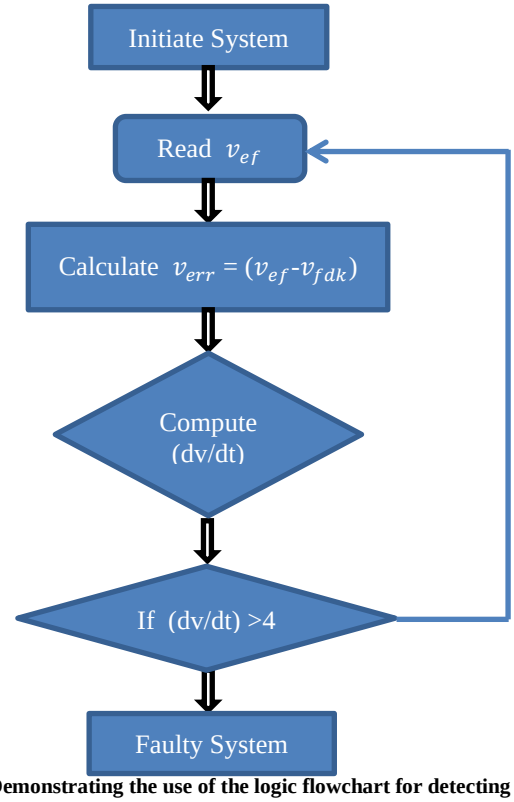


**Fig. 4 Demonstrating the use of the logic flowchart for detecting faults in the speed transducer**

Significant deviations of the estimated speed reference $\upsilon_{ef}$ from the feedback speed $\upsilon_{fdk}$ are associated with speed sensor failure, provided this deviation is beyond some threshold. For speed sensor fault detection purposes, the system analyzes the voltage change rate above an arbitrary threshold of 4 concerning the ratio of the absolute speed error to the nominal speed, also called the speed index.

### *4.3. Detecting Malfunction within Current Sensor*

Clarke transformation or α-β transformation is performed to reduce the analysis of three-phase systems by means of a two-phase equivalent. The mathematical concept is useful in the case of current sensor fault detection applications, e.g., induction motors. Investigating the two-phase current components makes the abnormalities or changes away from normal more pronounced, indicating a possible sensor malfunction. This provides a clearer insight into the behavior of currents in the stator, thus aiding in diagnosing faults.

This configuration of the motor system requires three current sensors to measure the S, R, and T phases accurately. Just like a voltage sensor's failure, the current sensor's failure causes erroneous gain or unwanted DC components. Thus, α-β-0 equations in voltages and currents can be written as follows:

With the Inverse Clarke transformation, the α-β two-phase system is expressed on the reference frame aligned with rotor flux, adding rotor angle (θ) to form the d-q coordinate system. The equations are as follows:

$$\begin{vmatrix} p \\ q \\ p_0 \end{vmatrix} = \begin{vmatrix} v_\alpha & v_\beta & 0 \\ -v_\beta & v_\alpha & 0 \\ 0 & 0 & v_0 \end{vmatrix} \begin{vmatrix} i_\alpha \\ i_\beta \\ i_0 \end{vmatrix} \quad (6)$$

$$\begin{vmatrix} i_\alpha \\ i_\beta \\ i_0 \end{vmatrix} = \sqrt{\frac{2}{3}} \begin{vmatrix} 1 & -1/2 & -1/2 \\ 0 & -\sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{vmatrix} \begin{vmatrix} i_a \\ i_b \\ i_c \end{vmatrix} \quad (7)$$

$$\begin{vmatrix} v_\alpha \\ v_\beta \\ v_0 \end{vmatrix} = \sqrt{\frac{2}{3}} \begin{vmatrix} 1 & -1/2 & -1/2 \\ 0 & -\sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{vmatrix} \begin{vmatrix} v_a \\ v_b \\ v_c \end{vmatrix} \quad (8)$$

With the Inverse Clarke transformation, the α-β two-phase system is expressed on the reference frame aligned with rotor flux, adding rotor angle (θ) to form the d-q coordinate system. The equations are as follows:

$$\begin{vmatrix} i_{sd} \\ i_{sq} \end{vmatrix} = \begin{vmatrix} cos(\theta) & sin(\theta) \\ -sin(\theta) & cos(\theta) \end{vmatrix} \begin{vmatrix} i_\alpha \\ i_\beta \end{vmatrix} \quad (9)$$

$$i_\alpha = i_{sd}cos(\theta) - i_{sq}sin(\theta) \quad (10)$$

$$i_\beta = i_{sd}sin(\theta) + i_{sq}cos(\theta) \quad (11)$$

This transformation changes the d-q phase vector from a rectangular coordinate system into an α-β two-phase representation, where certain formulas determine the angle θ. In this way, the conversion is again made from the α-β orthogonal two-phase way back into the conventional three-phase way according to these equations:

$$i_a = i_\alpha \quad (12)$$

$$i_b = \frac{-i_\alpha + \sqrt{3}i_\beta}{2} \quad (13)$$

$$i_c = \frac{-i_\alpha - \sqrt{3}i_\beta}{2} \quad (14)$$

When the current equations are transformed from the (a, b, c) frame to α-β-0 reference system, there stands different orthogonal coordinate framework:

$$i_b = (2/3)i_\alpha - 1/3(i_b - i_c) \quad (15)$$

$$i_\beta = \frac{2}{\sqrt{3}}(i_b - i_c) \quad (16)$$

$$i_0 = 2/3(i_a + i_b + i_c) \quad (17)$$

In this representation, the currents exist in an orthogonal reference system exhibiting symmetrical components. In applications absent of homopolar components, the original three-phase input signal may be expressed in terms of the space vector approach. Here, when dealing with phase currents, what is summed is all three phase currents, which then convert onto a, b, and c reference frames following the relationship:

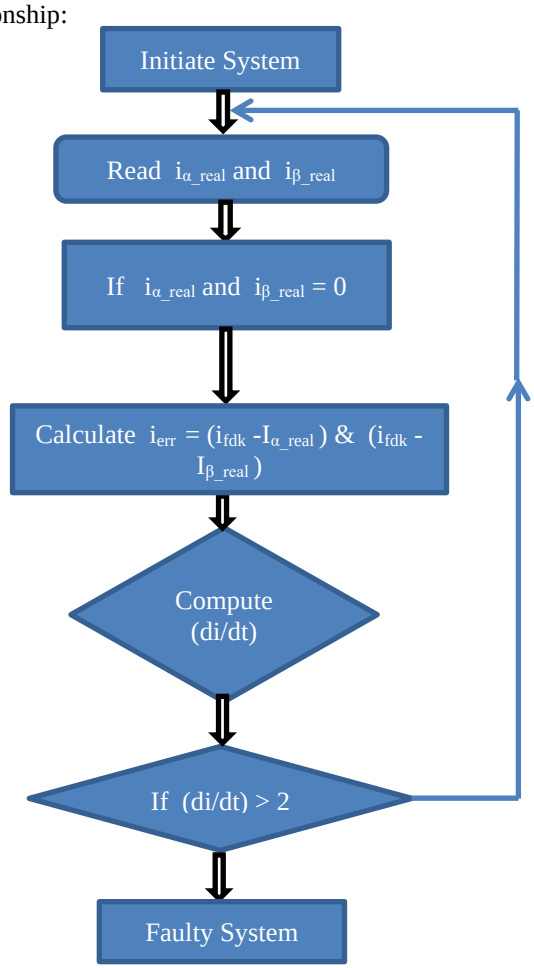


**Fig. 5 Demonstrating the use of the logic flowchart for identifying faults in the current transducer**

$$i_\alpha = i_a \quad (18)$$

$$i_\beta = \frac{i_\alpha + 2i_b}{\sqrt{3}} \quad (19)$$

$$i_a + i_b + i_c = 0 \quad (20)$$

To protect the current sensor failures in the system, the threshold limit for over-current detection is when the rate of change of the current value concerning time exceeds 2. Figure 5 shows the logical flowchart of the current sensor failure protection system against overcurrent.

Under fault conditions, the defective current sensor gives incorrect feedback. As such, the amplitude of the current in the α-β frame is abnormally large. When in phase 'a', the current sensor fails, the discrepancies between the feedback current and the value of the real current are quite significant and exceed the threshold limit.

$$i_{err} = i_{fdk} - i_{\alpha\_real} \quad (21)$$

$$i_{err} = i_{fdk} - i_{\beta\_real} \quad (22)$$

## 5. Results and Discussion

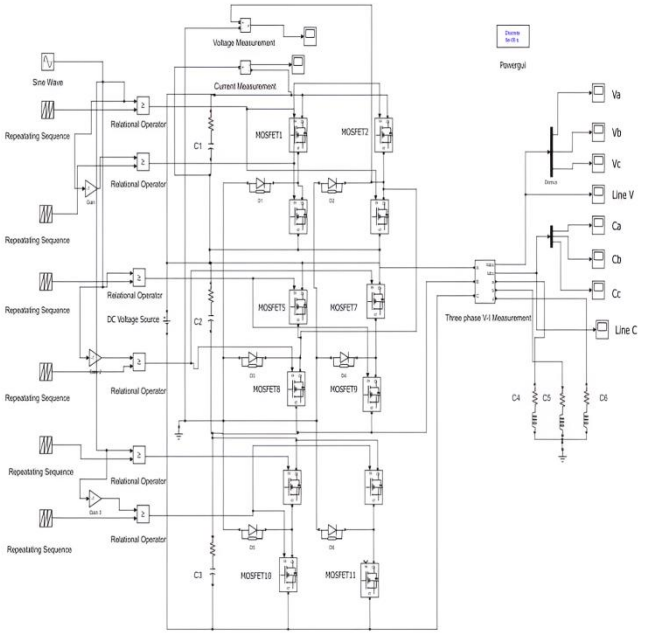


**Fig. 6 Simulation circuit diagram for a multilevel inverter supplying an (R-L) load**

Two types of fault conditions in MOSFET-based power electronic components were examined. Fault configurations in multilevel inverters were simulated in MATLAB and shown in block diagrams, as in Figure 6. The most significant is a short circuit due to the failure of the transistor, and the other is when any MOSFET is open-circuited, and the circuit is cut off. Analysis of the variation in Total Harmonic Distortion (THD) under normal and faulty conditions was also undertaken using a MATLAB FFT analyser.

Various scenarios were considered to justify and understand the implications of these faults. Those are scenario I, the lower arms of the MOSFETs transistor are isolated due to power failure detected in the unit; scenario II, the lower arms of MOSFETs are short-circuited because of a sudden current surge; scenario III, the upper arms of MOSFETs are isolated or disconnected as a consequence of

voltage discrepancies and lastly scenario IV, the upper arms of MOSFETs are short-circuited. These four scenarios are depicted in Figure 7.

Figure 8 represents the output voltage at the load under normal operating conditions in a valid phase. The output voltage signal variations under the above-mentioned fault conditions are shown.

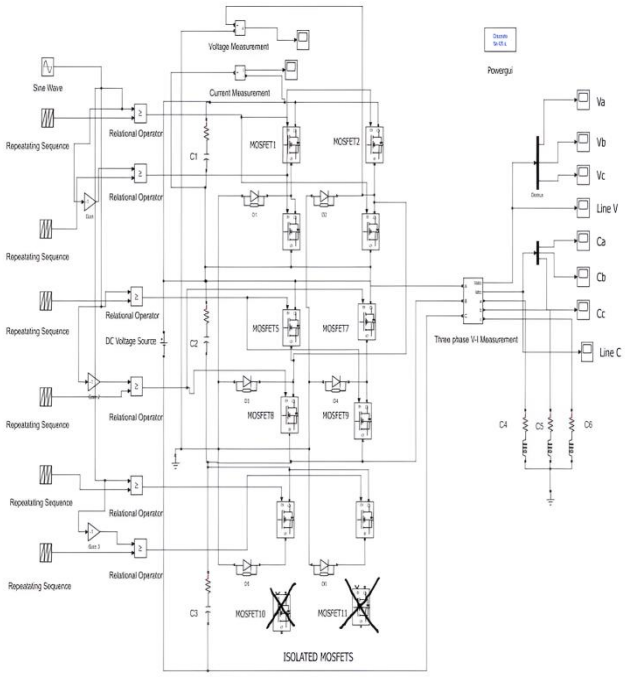


**Fig. 7(a) The block diagram showcasing isolated lower arm MOSFET transistor faults of a multilevel inverter**

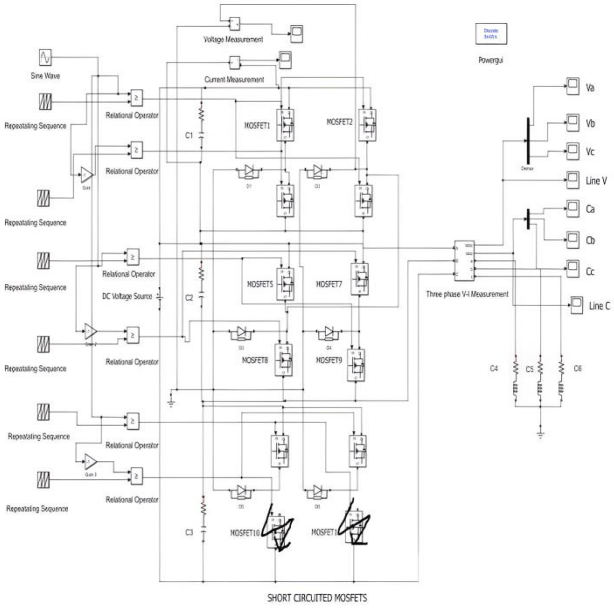


**Fig. 7(b) The block diagram showcasing short-circuited lower arm MOSFET transistor faults of a multilevel inverter**

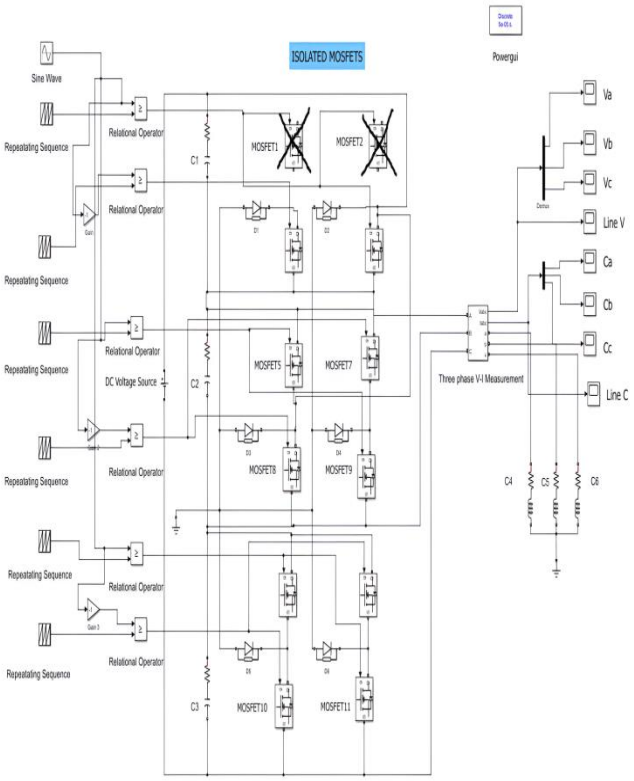


**Fig. 7(c) The block diagram showcasing isolated upper arm MOSFET transistor faults of a multilevel inverter**

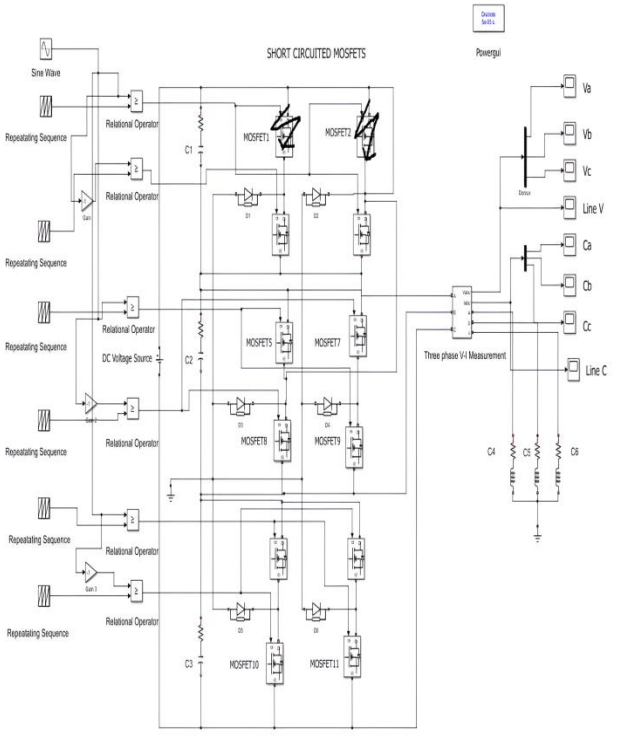


**Fig. 7(d) The block diagram showcasing short-circuited upper arm MOSFET transistor faults of a multilevel inverter**

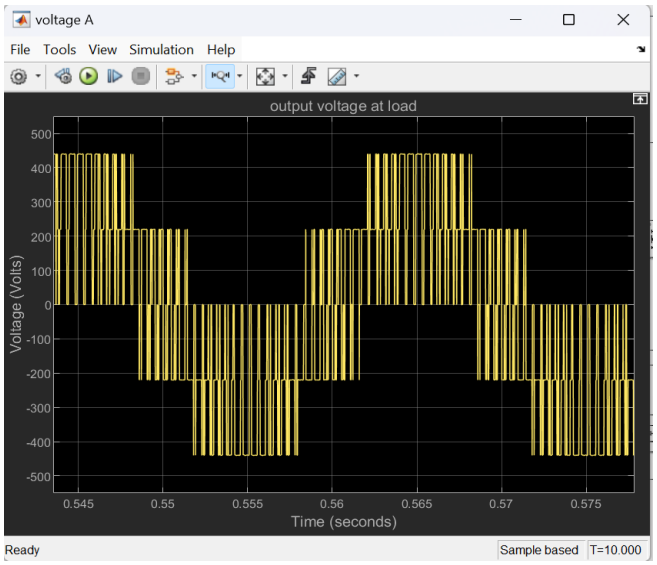


**Fig. 8 Output voltage signal functioning under normal operating conditions supplying an R-L load**

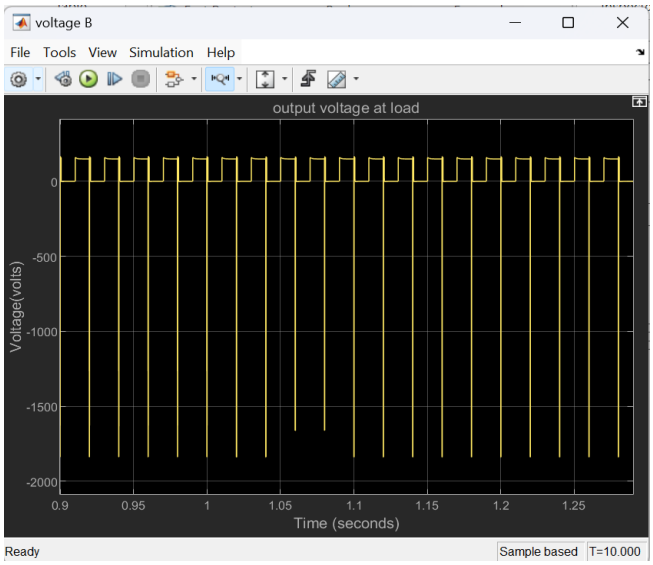


**Fig. 9 Output voltage when lower arm MOSFETs are isolated in an R-L load configuration**

In Figure 9, the output loads voltage waveform is represented under the isolation of the lower arm MOSFETs. Thus, you can see that the output voltage does not follow the sinusoidal pattern very closely and shows asymmetrical signal behavior. Because of the failure of the power transistor, that unit would no longer participate uniformly with other power components.

This way, near the positive cycle of the signal, it is suppressed almost entirely, whereas the negative cycle encounters severe over-voltage to the extent of nearly four times that of the input DC voltage source.

If a fault occurs because of a short-circuited transistor, the output voltage signal becomes deeply asymmetrical. Due to transistor failure, the voltage signal in the positive cycle has gone over by almost two times the normal DC link voltage, with some sample periods missing in the negative half cycle due to a transducer malfunction. Figure 10 illustrates the voltage variation when MOSFETs experience a short circuit.

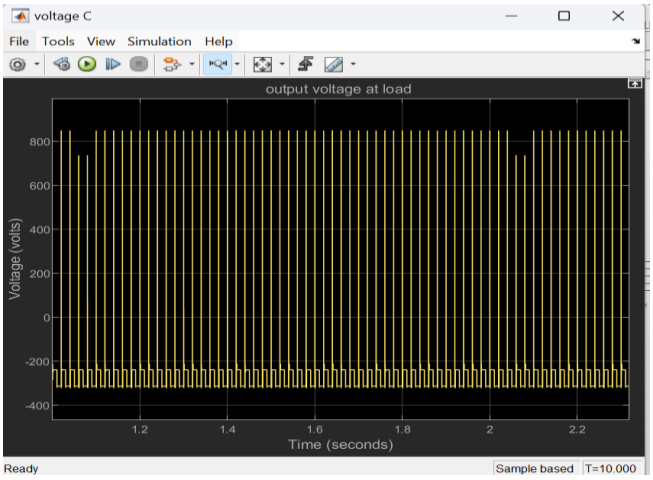


**Fig. 10 Output voltage signal when the lower arm MOSFETs are in a short circuit supplying R-L load**

Figure 11 depicts when MOSFETs in the upper arm are isolated due to power transistor failure in that unit, and a sudden voltage overload in the positive half cycle (about three times the input DC link) is observed. As a result, the signal behaves extremely asymmetrically, and the negative cycle is completely attenuated.

Figure 12 represents the output voltage variation when the upper-arm transistors are short-circuited in an R-L load at a multilevel inverter. So, the positive half-cycle is completely filtered out, and the negative half-cycle operates within the normal range of the DC link voltage, but the step signal is offset to zero, and the DC component is homopolar.

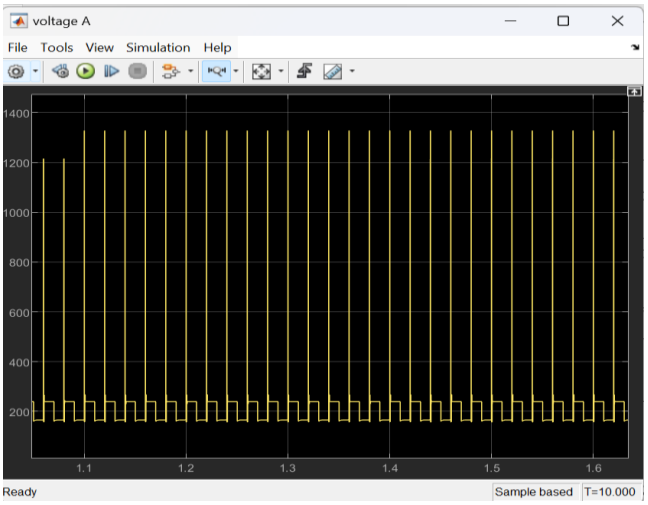


**Fig. 11 Output voltage signal when the upper arm MOSFETs are isolated in an R-L load**

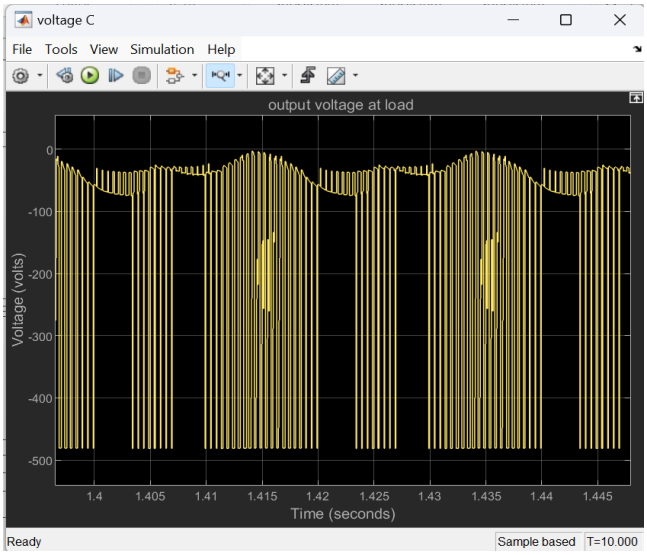


**Fig. 12 Output voltage signal when the upper arm MOSFETs are short-circuited in an R-L load**

In this analysis, the Fast Fourier Transform (FFT) was applied to examine the behavior patterns of output voltages under faulty conditions. The Total Harmonic Distortion (THD) values were determined using an FFT analyzer.

By comparing the THD values between the valid system and faulty phases, it validated the detection and severity of each fault. Ideally, the THD value is desired to be as low as possible for smooth operation. An increase in THD value indicates the severity of each fault condition.

Figure 13 illustrates a comparative FFT analysis of THD values of output voltages under various operating conditions such as (a) valid phase, (b) lower arm MOSFETs become isolated, (c) lower arm MOSFETs are short-circuited, (d) upper arm MOSFETs become isolated, and (e) upper arm MOSFETs short-circuited. Through this analysis, it was observed that the amplitude of the fundamental frequency in the valid phase was significantly higher about (more than three times) in comparison to different fault conditions, and the THD value in the valid phase was remarkably lower approximately (about 67%) compared to the faulty conditions. THD values in fault conditions are quite high, so the severity of each faulty phase is notable. THD values across different faults were very similar.

This methodology provides more accuracy in terms of THD values and better AC signal quality due to observing various fault conditions (as mentioned in Figure 7) with multiple parameters like short circuit MOSFETs, isolated MOSFETs, and multiple switch failures.

Thus, it is an effective and reliable fault detection method, as shown in the difference in THD values from normal to fault conditions, which is quite significant.

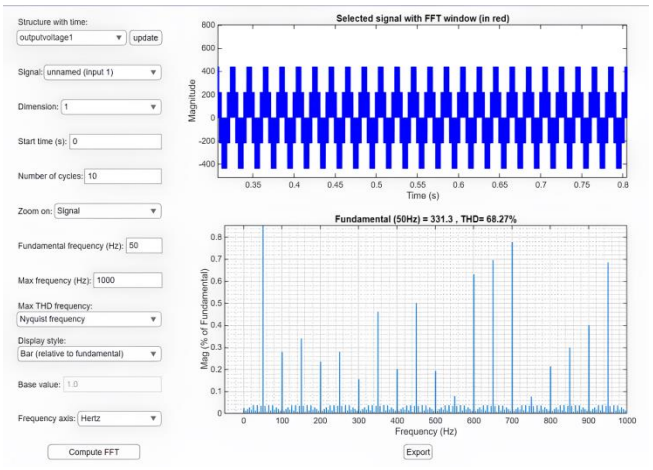


**Fig. 13 (a) Under Valid Phase**

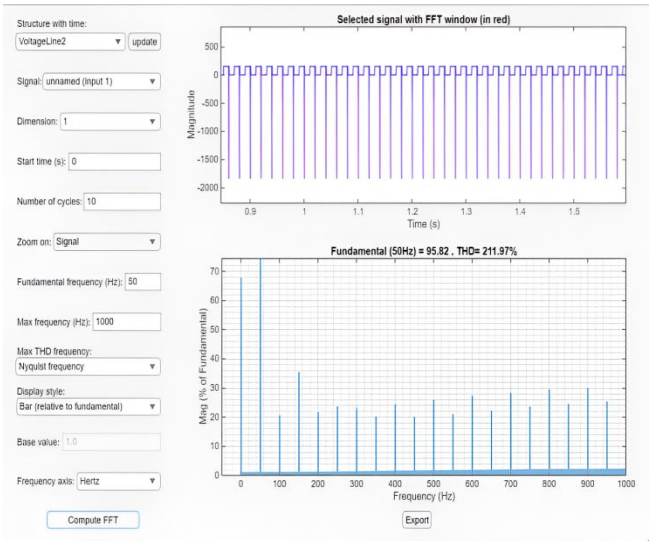


**Fig. 13(b) The lower arm MOSFETs are isolated**

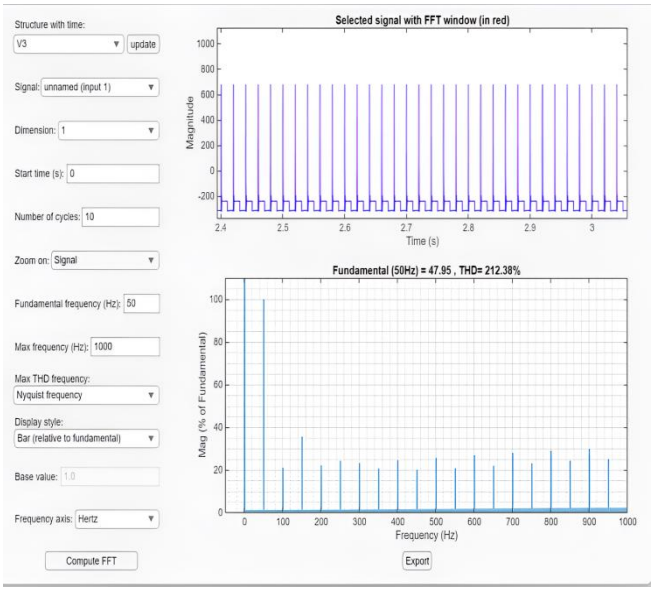


**Fig. 13(c) The lower arm MOSFETs are short-circuited**

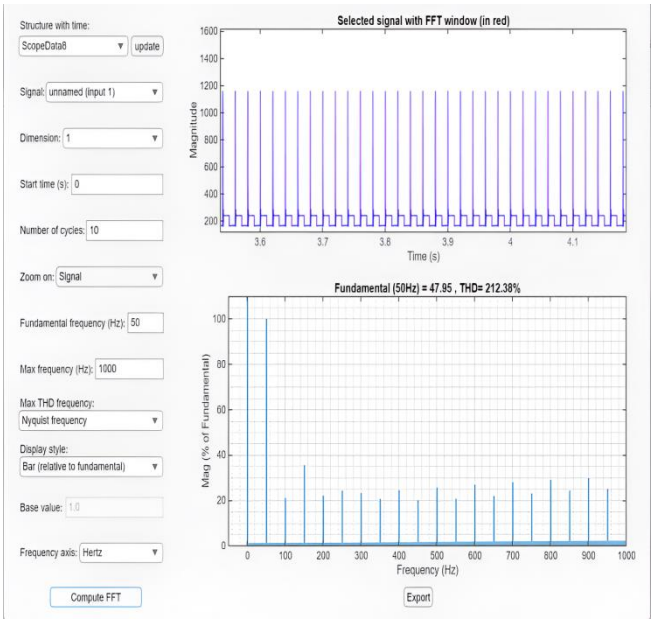


**Fig. 13(d) The upper arm MOSFETs are isolated**

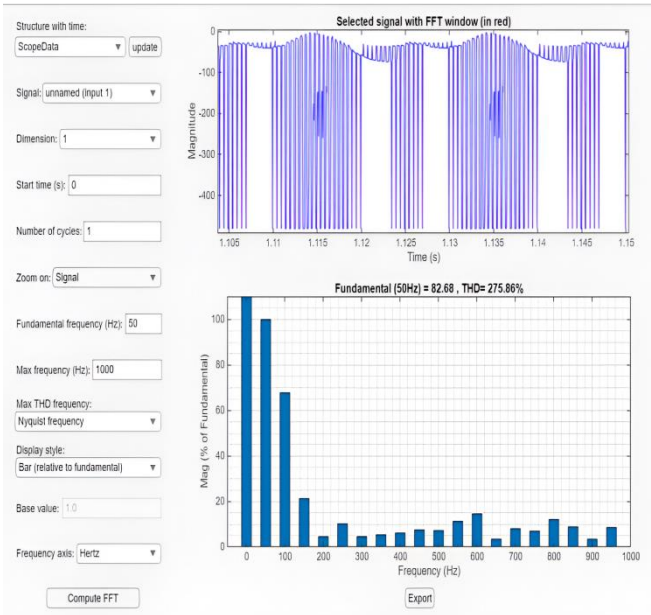


**Fig. 13(e) The upper arm MOSFETs are short-circuited**

Figure 14 portrays the fluctuation occurring within the load current due to the multifarious level inverter system working under normal operations, where the output AC signal is symmetrical.

The figure denotes the change of load current subject to 2 fault conditions when one device off the electrical power converter, e.g. a MOSFET in a multilevel inverter (Figure 15), is disconnected and when there is short-circuiting (Figure 16). The Current waveform in both cases will be distorted from a pure sinusoidal shape; nevertheless, the current values seem to stay less affected overall. In the case of connecting the transistor, the minus half cycle of the current waveform will show less reduction compared to short-circuiting the component concerning normal operation conditions.

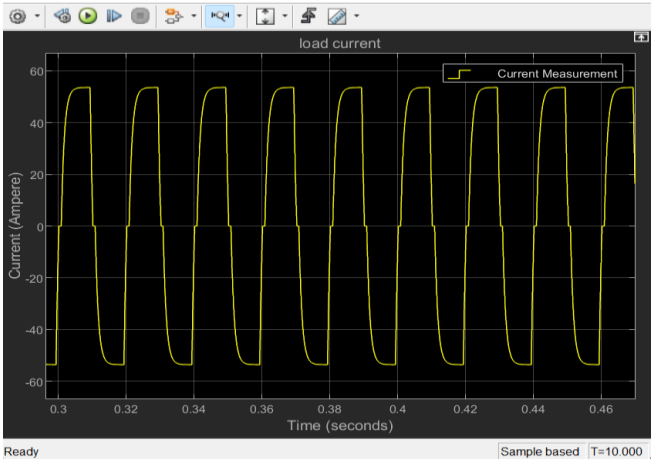


**Fig. 14 Difference of Output load current under normal operating conditions**

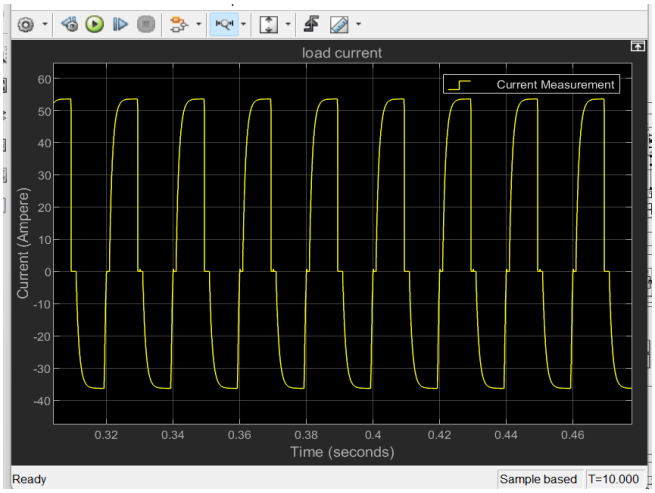


**Fig. 15 Difference of Output load current when MOSFETs are isolated**

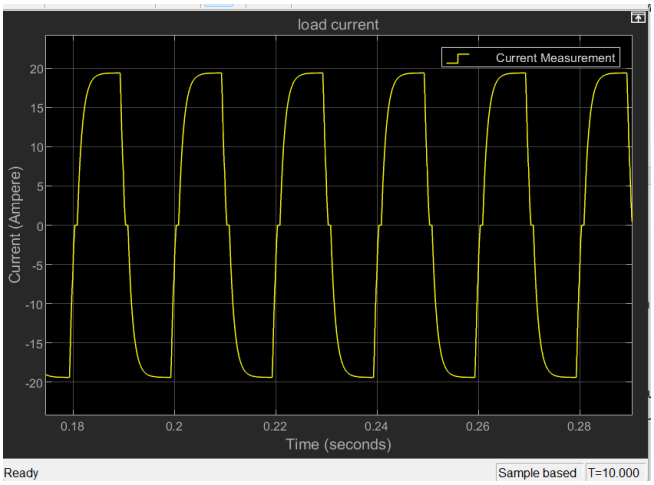


**Fig. 16 Difference of Output load current when MOSFETs experience short circuit**

## 5. Conclusion

Seamless interaction between smart grid units is vital for system reliability. Converters should be able to receive fault announcements straight away from any load, thus saving the entire system from probable failure. This study finds that faults in multilevel inverters can result in severe damage to interconnected power equipment components.

Isolating a transistor causes the waveform to depart from its sinusoidal characteristics toward asymmetrical, with overvoltage spikes during short-circuit conditions. In addition, various sample intervals are subjected to attenuation or complete suppression across both half cycles, causing deep system defects. These failures can initiate power outages, with the most catastrophic cases being the instant tripping of the inverter power system.

Additionally, FFT analysis reveals that the Total Harmonic Distortion (THD) values during fault conditions are much higher than those during normal operation, which indicates a significant deviation from standard waveform integrity.

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